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RELIABILITY STUDIES OF APPLICATION SPECIFIC INTEGRATED CIRCUITS OPERATED AT CRYOGENIC TEMPERATURE

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ABSTRACT

Cold electronics has become a key technology in many areas of science and technology including space exploration programs and particle physics. A major experiment with a very large number of analog and digital electronics signal processing channels to be operated at cryogenic temperatures is the next generation neutrino experiment, the Deep Underground Neutrino Experiment (DUNE). The DUNE detector uses liquid Argon at 87K as a target material for neutrinos. The DUNE electronics [1] consists of custom-designed ASIC (Application Specific Integrated Circuits) chips based on low power 180 nm-CMOS technology. The main risk for this technology is that the electronics components will be immersed in liquid argon for many years (20-30 years) without access. Reliability issues of ASICs may arise from thermal stress, packaging and manufacturing related defects: if undetected those could lead to long-term reliability and performance problems. The scope of this paper is to explore non-destructive evaluation techniques for their potential use in a comprehensive quality control process for during prototyping, testing and commissioning of the DUNE cold electronics system.

Keywords: Liquid Argon, correlation, cryogenic, neutrino, DUNE, NDE

NOMENCLATURE

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1. INTRODUCTION

The Liquid-argon technology-based Time Projection Chambers (LAr-TPC) for DUNE offer a unique opportunity to address two major goals in the neutrino physics, a measurement of CP-violation and to determine the neutrino mass hierarchy [3]. A LAr-TPC contains a modular electronics system with 3,000 Front-End Mother Boards (FEMBs). Each FEMB provides for the signal processing of 128-channels (wires) and may host of up to 18 ASICs bringing the total number of ASICs to ~ 50,000 per LAr -TPC. Functionally, these chips include amplifier, signal shaping, digitizer and data assembly functions. Data transmission is achieved via a serial copper cold cable at transmission speeds of 1 Gb/s. CMOS technology is well suited for operation at cryogenic temperature, due to its low power usage and minimal heating of the cryogenic liquid, thereby reducing the formation of bubbles in the detector. CMOS failure mechanisms, such as hot-carrier effect, and dielectric breakdown at cryogenic temperature can be minimized by tuning the operating voltages and were discussed by [2]. Detailed lifetime studies can be found in [4][5].

Scanning Acoustic Microscopy (SAM) is a powerful non-destructive evaluation technique for inspection of microelectronics integrated circuit packages [6]. The integrated circuits are made from composite materials and are susceptible to thermally induced stress. A such induced discontinuity inside the chip might affect the reliability of an integrated circuit and could cause long-term performance problems [6]. In addition to the SAM technique, we have also used X-ray microscopy to inspect chip internal wire-bond, broken wire-bonds and solder defects. Not all defects are sensitive to both X-ray and SAM, it depends on the nature of the defects [7].

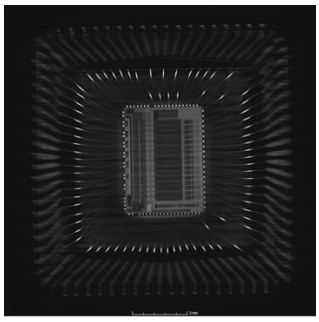

Figure 1: **X-ray micrograph image of an ASIC, the wire-bond and the internal structure are clearly visible, the spatial resolution of the instrument is 10 μm.**

2.MATERIALS AND METHODS

SAM uses ultrasound to interrogate a material by focusing periodic sound waves onto a small region of a sample. The signal will be a function of the acoustic impedance of the different material layers. Figure 2 represents an example of a reflected signal waveform. In order to probe the material sufficiently deep with good resolution one has to select an optimum frequency. We

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chose the frequency of 15 MHz and a focal length of 2 inches for our measurements.

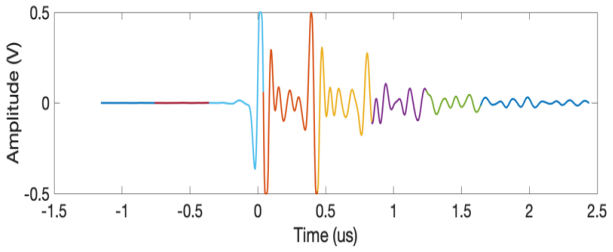

Figure 2: **An example of reflected wave signal. Each color represents different depth in the sample**.

The ASIC chips tested here are about 1 mm thick and 2cm x 2 cm wide and includes about 320,000 transistors. The beam profile of the scan has a width of 250 μm and the step size is 125 μm, which ensures that every point on the AISC is scanned.

2.1 The Correlation Analysis Strategy

A correlation analysis has been developed to study the similarities in the chips' internal materials structure within a group of ASICs. The signals are collected from each and every point on an ASIC, the scans yield a 150 x150 matrix of A-Scans, containing 22,500 pixels/chip in total. In order to compare two ASIC chips for any structural differences, we calculate a cross-correlation value for each pixel based on the two corresponding A-Scans by quantifying similarity of their time traces over a given time window. Effectively we compare two ASIC chips at each position and thereby generate a 2-D image. A low correlation value from the outside pins of ASICs are expected due to the distortions of the reflections from the edges (edge-effect) [8].

$$\Phi_{ab} = \frac{\sum_{i=1}^{n} a_i b_i}{\sqrt{\sum_{i=1}^{n} a_i^2 \sum_{i=1}^{n} b_i^2}} \qquad (1)$$

The correlation coefficient for two different ASICs is defined according to equation (1). Here a_i, b_i refer to the reflected waveforms in time bin i detected with the transducer at the scanned location on the two different ASICs. These waveforms are in digitized format, recorded with a sampling time scale of 40 ns, slightly oversampling the 15 MHz pulsed acoustic signals. Correlation value Φ_{ab} quantifies similarity between the two waveforms over a chosen time window, corresponding to n time samples, and a specific depth regime inside the chips. In this analysis we made certain that the starting time of all the incident waveforms used are synchronized, to ensure that there is no offset – as would be indicated by a time lag between the incident waves reflected off the top surface of the sample. The resulting correlation values Φ_{ab} computed yield a 2-D map/image of the chip comparison. If the reflected waveforms of the two chips are close to identical, we expect a high correlation value close to 1. Correlation value of 0 indicates no correlation and -1 corresponds to a phase shift between in the waveforms from the two chips.

3.RESULTS AND DISCUSSION

Images were created by forming the correlation values for the entire time window, and a select narrowed time-window to focus on a given depth inside the material. Figure 3, shows the image formed using the correlation values for two different ASICs

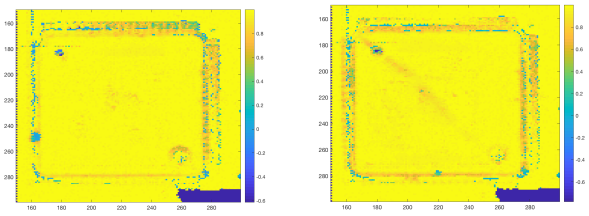

Figure 3: **In the left we show the correlation map of two similar ASICS. It can be seen that there are no substantial differences inside the chip. To the right we show two ASICs that show substantial differences along a diagonal line, related to a difference inside the packaging of the circuitry.**

The correlation analysis was also done in the frequency domain by taking the Fourier transform of the signal, and the features appeared to be the same.

A more general view of a collection of 9 ASICs and their internal structural similarities can be gleaned from Figure 4. Here, a distribution of the correlation values is shown for 8 chips compared to a reference chip. As can be seen most chips show correlation value distributions clustered around 1, corresponding to a high level of similarity of the inner structure when compared with the reference chip. One sample (chip identification number 1745) exhibits a very broad correlation value distribution. This chip had been purposely exposed to mechanical pressure to induce delamination inside.

One of the key motivations for this study is to determine if any structural changes inside the ASICs' composite material occurs as a result of temperature cycling between room temperature and submersion in liquid nitrogen. In these tests several ASIC chips were immersed in liquid nitrogen followed by an acoustic microscopy scan done immediately after they were taken out. The summed amplitudes of the acoustic scans (C-scan) for one of chip comparing the 2-D images before (left) and after (right) the temperature cycling is shown in Figure 5. There is an apparent difference in the internal structure as indicated in the Figure 5. A small strip feature appeared at a depth of 0.4 mm inside the ASIC package (calculated from the time of the reflected wave, the velocity of the sound in this composite material is taken as 2800 m/s) [9].

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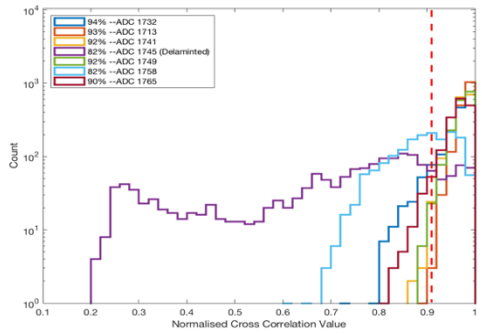

Figure 4: **The Distribution of the correlation values for the damaged ASIC is compared with the other ASICs**.

To gain a more detailed view of the regions of interest, we show in Figure 6 the corresponding B-Scan images of the chip before (top) and after the liquid nitrogen treatment (bottom). The comparison shows a clear change in the center region. It appears that a multi-layer indentation was already present before the temperature cycling (top), and is much enlarged after the cycling (bottom).

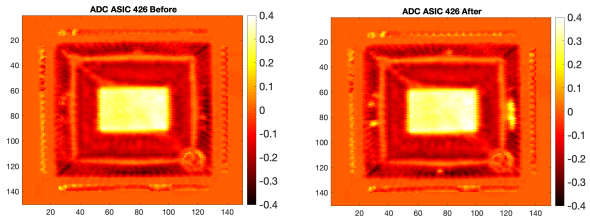

Figure 5: **The C-Scan image of the IC Before (left) and after (right) treated with the liquid nitrogen, there is a change observed in the sample**.

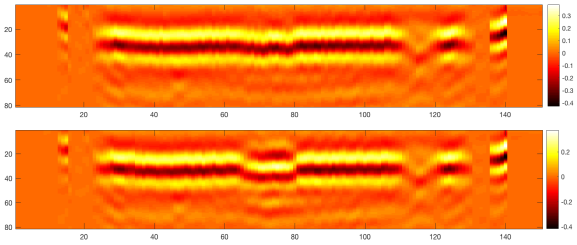

Figure 6: **The B-Scan image from the IC before (top) and after (bottom) treated with the liquid nitrogen for 20 minutes.**

CONCLUSIONS

In this work we have developed a correlation analysis allowing one to perform a comparison between different ASIC samples. For example, one can compare statistical samples of chips with different testing history, such as failed functional tests and well performing chips. In some of the chip samples we were able to identify a diagonal feature across the inner chip at the depth of the thermal paste layer.

Furthermore, this correlation analysis was used to study the effects of temperature cycling between 87K and room temperature. Our results demonstrate structural changes in a few chips that occurred after cryogenic cycling. Additional studies are underway to evaluate the impact of these structural changes including X-ray imaging of wire bonds. Finally, we are also planning to perform functional tests and destructive evaluation to fully understand the origin of these structural changes.

ACKNOWLEDGEMENTS

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